REMARKS

Claims 1, 8, 17, 19, 20, 33 and 39-42 have been amended. Claims 12-14 and 23 have been canceled. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 40-41 stand rejected under 35 U.S.C. § 112, second paragraph. The rejection is respectfully traversed. Claims 40 and 41 have been amended to address the concerns raised in the Office Action. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 1-10, 12-14, 17, 19-23, 33-35 and 39-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 7,002,823 (Ichiriu) in view of U.S. Patent 6,944,039 (Nataraj). Applicant respectfully traverses these rejections.

Claim 1 recites a method for testing a memory device. The method comprises "disconnecting all match lines of said memory device from a priority encoder of said memory device; confirming proper operation of a control line used to enable output from a match line under test; [and] connecting an output from the match line under test to the priority encoder." Applicant respectfully submits that the cited combination fails to teach or suggest these limitations.

The Office Action has manipulated the teachings of the cited combination to read on resetting and enabling acts of the claimed invention (prior versions of the above limitations). Applicant has disputed the Office Action's reading of the cited combination in prior responses and chooses not to repeat those arguments here. Although Applicant maintains that the prior version of claim 1 was allowable over the cited art, Applicant has clarified the language of the above limitations in response to the Examiner's statements in the Office Action. Ichiriu and Nataraj merely teach precharging their match lines, *Ichiriu, col. 6, line 65; Nataraj, col. 5, lines 30-31*, the purpose of which is to bring each match line to "a high logical level at the start of a comparison operation [to then allow each line to be] pulled down to a low logical level" in the event of a mismatch. *Ichiriu, col. 6, lines 65-66.* Applicant respectfully submits that this is not the same as "disconnecting all match lines of said memory device from a priority encoder" and "connecting an

output from the match line under test to the priority encoder." These features are simply not found in the cited combination.

Next, Applicant maintains that the Ichiriu and Nataraj combination fails to teach the act of confirming proper operation of a control line used to enable output from a match line under test for the reasons presented in Applicant's October 17th Amendment. Moreover, claim 1 also recites the acts of "comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." The Ichiriu and Nataraj combination fails to teach or suggest these limitations, particularly, neither reference teaches the act of confirming the operation of the device based on an expected result whereby "said expected result compris[es] an expected match indication on the match line under test." This feature is simply not disclosed in the cited combination.

For example, Ichiriu does not teach comparing the result of the search operation with an expected result. Ichiriu teaches validity bits that record whether the data in a given row is valid. *Ichiriu, col. 7, lines 65-67, col. 8, lines 1-5.* These validity bits are used in Ichiriu to prevent matches asserted on invalid rows, *Ichiriu, col. 8, lines 18-31*, or to determine whether the result of a search operation is invalid because a match may have been asserted on an invalid row. *Ichiriu, col. 23, lines 19-25.* The validity bits, however, are not used to compare the result of the search operation with an expected result, whereby the "expected result" comprises an "expected match indication" of the match line under test. On the contrary, a search operation involving an invalid row can still output an expected result – invalid, but expected. Ichiriu also teaches parity testing for each row, but this tests for parity during a read operation and does not test a search operation against an expected result. *Ichiriu, col. 8, lines 34-45.*

Also, Nataraj teaches methods affecting the timing of compare operations in a test mode, not comparing the result of a compare operation with an expected result. *Nataraj, col. 4, lines 42-*

57. Therefore, neither Ichiriu nor Nataraj teach nor suggest comparing the result of a search operation with an expected result whereby "said expected result compris[es] an expected match indication on the match line under test," confirming proper operation based on whether the result is equal to the expected result, or indicating an error if the result is not equal to the expected result. This is one more reason why claim 1 is allowable over the cited combination.

Claims 2-7 depend from claim 1 and are allowable along with claim 1 for at least the reasons set forth above and on their own merits.

Claim 8 recites "connecting said match line of the set of memory cells being tested to a priority encoder of the memory device" and "disconnecting match lines of other sets of memory cells from the priority encoder." As such, claim 8 is allowable for at least the reasons set forth above and on its own merits. Claims 9 and 10 depend from claim 8 and are allowable along with claim 8.

Claim 17 recites "enabling circuitry that connects a match line to a priority encoder to provide said match signal as an output when said set of memory cells is being tested, said enabling circuitry connecting the match line after disconnecting all match lines of the memory circuit and confirming proper operation of a control line." As such, claim 17 is allowable for at least the reasons set forth above and on its own merits. Claim 19 depends from claim 17 and is allowable along with claim 17.

Claim 20 recites "for each set of memory cells, enabling circuitry that connects a match line to a priority encoder of the memory device to provide said match signal as an output when said set of memory cells is being tested" and "a word line that selects said set of memory cells, said enabling circuitry connecting said match line in response to a signal on said word line, said enabling circuitry connecting the match line after disconnecting all match lines of the memory circuit and confirming proper operation of a control line used to generate the signal on the word line." As such, claim 20 is allowable for at least the reasons set forth above and on its own merits. Claims 21 and 22 depend from claim 20 and are allowable along with claim 20.

Claim 33 recites "for each set of memory cells, enabling circuitry that connects a single match line to a priority encoder to provide said match signal as an output when said set of memory cells is being tested" and "a word line that selects said set of memory cells, said enabling circuitry connecting said single match line in response to a signal on said word line." As such, claim 33 is allowable for at least the reasons set forth above and on its own merits. Claims 34 and 35 depend from claim 33 and are allowable along with claim 33.

Claim 39 recites "for each set of memory cells, enabling circuitry that connects a single match line to a priority encoder to provide said match signal as an output when said set of memory cells is being tested" and "a word line that selects said set of memory cells, said enabling circuitry connecting said single match line in response to a signal on said word line." As such, claim 39 is allowable for at least the reasons set forth above and on its own merits. Claims 40 and 41 depend from claim 39 and are allowable along with claim 39.

Claim 42 recites "disconnecting all match lines of said memory device from a priority encoder of said memory device" and "connecting said match line under test to the priority encoder." As such, claim 42 is allowable for at least the reasons set forth above and on its own merits.

In addition, Applicant reasserts that the Office Action has failed to provide a proper analysis under the Graham factors for at least the reason set forth in Applicant's October 16th Amendment.

Accordingly, the rejection should be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: March 26, 2008

Respectfully submitted,

By _____

Gianni Minutoli
Registration No.: 41,198
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant